REMARKS

Claims 1, 3-53 are currently pending in the subject application and are presently under consideration.

Favorable reconsideration of the subject patent application is respectfully requested in view of the comments herein.

I. Rejection of Claim 1 Under 35 U.S.C. §112, First Paragraph

Claim 1 stands rejected under 35 U.S.C. §112 as failing to comply with the written description requirement. Withdrawal of this rejection is respectfully requested for at least the following reasons. The specification discloses in full, clear, concise, and exact terms that which can enable one to carry out the claimed subject matter.

At page 8 of the Final Office Action (mailed December 27, 2007), the Examiner contends that there is no disclosure within the specification or original claims for a time synchronization apparatus that "is configurable to operate as both a synchronization master and a synchronization slave" as recited in independent claim 1. It is readily apparent that support for these features is disclosed in numerous portions of the specification. "For example, the Synchlink circuit or chip 314 is configurable by the host processor 302 to operate the synchronization module 300 as ***a synchronization master or a synchronization slave***." (*See* pg. 37, ll. 9-11; *see* also pg. 17, ll. 1-10). Clearly, there is support for a single component (*e.g.*, the synchronization apparatus) that is configurable to operate as a master, and also configurable to operate as a slave. Therefore, it is illogical to suggest that this component cannot be configurable to operate as both.

The Examiner freely admits that there is support for the apparatus to act as either a master or a slave, but tacitly ignores that if the claim language actually recited "an apparatus that is configurable as either a master or a slave" then a hypothetical prior art reference that taught an apparatus that is configurable as a master (but not a slave) or a slave (but not a master) would still read on the claim, even though the prior art only teaches a single configurable state while applicants' specification (and the claimed subject matter) clearly recites that the apparatus can be configurable as both. Applicants have adequate disclosure for such and have selected to narrow the scope of the claim to suitably prevent such broad interpretation. It is unconditionally illogical to accept that the apparatus can be configurable as a master and also configurable as a slave (as the Examiner concedes), but then reject that the apparatus can be configured as both.

If, as the Examiner maintains, there is no support for the apparatus to be configurable as both a master and a slave, then the Examiner must illustrate which of the two is not supported—otherwise, there is *de facto* support for "both." Yet, the Examiner has failed to show that the apparatus is not configurable as a master (in fact, the Examiner admits there is support for this), and further the Examiner has not shown that the apparatus cannot be configurable as a slave (again the Examiner admits there is support). Thus, there is support for a single apparatus that can do ***both***. In fact, the Examiner is not here rejecting what is claimed, but rather the Examiner is rejecting elements that are **not** claimed. The sole basis for this rejection is the Examiner's position that there is no support for the apparatus to be configurable as both ***at the same time***. Without the "at the same time" clause, the Examiner's argument is self-refuting, and such limitations are not found in the claim. That is, the claim does ***not*** recite "at the same time" and it is not clear what evidence the Examiner employs to determine the *ad hoc* addition of such limitations to the claim represents a reasonable interpretation of the claim.

Pointedly, it is impermissible for the Examiner to insert arbitrary limitations into the claim, and then argue applicants have not supported in their disclosure those arbitrary limitations invented by the Examiner. Yet, this is precisely what the Examiner has done here. Accordingly, this rejection should be withdrawn.

Moreover, the Examiner's analysis is continually inconsistent with respect to both the claims and the cited art, which obfuscates the issues and work against concise responses. For example, with respect to the present 35 U.S.C. §112 rejection, the Examiner refuses to read the term "both" of claim 1 on its face in favor of an arbitrary interpretation not found in the claim: "both at that same time." However, when comparing claim 1 to cited references under 35 U.S.C. §103 (see Final Office Action at pg. 9; see also §II, *infra*), the Examiner clearly reads the term "both" as "either one or the other" (otherwise the Yamanaka reference makes no sense) and does not include the "at the same time" addition, ostensibly because such an interpretation would even more clearly avoid the teachings of the cited art. While in both cases, the Examiner's interpretation of the claim is arbitrary and both depart from the actual claim language, it is respectfully requested that the Examiner settle on one interpretation of the claim rather than changing the interpretation based upon the type of rejection presented.

With regard to inconsistent use of the cited art, see §II, *infra*.

II. Rejection of Claims 1, 3-7, 13-28, 30-34, 38-46 and 48-53 Under 35 U.S.C. §103(a)

Claims 1, 3-7, 13-28, 30-34, 38-46 and 48-53 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka, *et al*. (US 4,807,259, hereinafter referred to as "Yamanaka") in view of Voth (US 6,199,169). It is respectfully submitted that this rejection should be withdrawn for at least the following reasons. Neither Yamanaka nor Voth, either alone or when combined, disclose all the claimed features. Moreover, Yamanaka and Voth produce an inoperative combination and/or do not yield a reasonable expectation of success to make the proposed combination. Therefore, these references are not permissibly combinable.

> To reject claims in an application under §103, an examiner must establish a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) ***must teach or suggest all the claim limitations***. In addition, ***there must be a reasonable expectation of success to make the proposed combination***. *See In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). "[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR v. Teleflex*, 550 U.S. ___, 127 S. Ct. 1727 (2007) *citing In re Kahn*, 441 F. 3d 977, 988 (CA Fed. 2006).
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> ***If references taken in combination would produce a "seemingly inoperative device," we have held that such references teach away from the combination and thus cannot serve as predicates for a prima facie case of obviousness***. *In re Sponnoble,* 405 F.2d 578, 587, 160 USPQ 237, 244, 56 C.C.P.A. 823 (1969) (references teach away from combination if combination produces seemingly inoperative device); *see also In re Gordon,* 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (inoperable modification teaches away). *McGinley v. Franklin Sports Inc.*, 262 F.3d 1339, 60 USPQ2d 1001, 1010 (Fed. Cir. 2001) (emphasis added).

The claimed subject matter relates generally to industrial control systems (*see, e.g.*, control system 50, FIG. 2) with a time synchronization apparatus (*see, e.g.*, S/L 82, FIG. 2) for synchronizing operation of a first controller (*see, e.g.*, controller 56, FIG. 2) with that of a second controller (*see, e.g.*, controller 54, FIG. 2). More specifically, the time synchronization apparatus can be configured to operate as either a master or a slave (and therefore a single

apparatus can be configurable as both), can synchronize across disparate and/or multiple time synchronization zones (*see e.g.*, pg. 12, line 15 – pg. 14, line 26) and can function in topologies other than a star topology such as a daisy chain or loop configuration, or combinations thereof (*see e.g.*, pg. 18, ll. 15-17). In particular, independent claim 1 recites, "a processor interface for interfacing the synchronization apparatus with a host processor, the time synchronization apparatus is ***configurable*** *to operate* ***as both*** *a synchronization master and a synchronization slave*." Similarly, independent claims 38 (and similarly claim 39 and 52) recites, "a synchronization circuit…***configurable*** by the host." Yamanaka does not disclose such features.

Yamanaka relates to a time synchronization method, wherein the time of a slave clock is synchronized with the time of a master clock. (*See* col. 7, ll. 6-49). The master clock resides in a master station (*see* element 17, FIG. 3A) and the slave clock resides in a slave station (*see* element 37, FIG. 3B). While Yamanaka discloses a method for time synchronization for a slave clock, the reference is silent as to whether either the master or the slave station is configurable. Accordingly, Yamanaka does not teach a time synchronization apparatus that is ***configurable to operate as both a synchronization master and a synchronization slave***. Rather, Yamanaka teaches a designated master station that synchronizes a designated slave station.

At page 9 of the Final Office Action, the Examiner incorrectly argues Yamanaka teaches these features by joining together two mutually exclusive scenarios. In the first case, the Examiner argues that the ***master station*** (or components thereof) is the synchronization apparatus to illustrate that the apparatus is a master, while in the second case, the Examiner argues the ***slave station*** is the synchronization apparatus to stand for the proposition that the apparatus is a slave, even though both of these components are clearly distinct from one another. Hence, the Examiner has defined the synchronization apparatus as the master station to reject a first portion of the claims and later defines the synchronization apparatus as the slave station to reject a second portion of the claims. Such analysis ignores the claimed features that the apparatus is configurable as both a master and a slave in favor of showing that both a master and a slave can exist in a system, which does not read upon the claims. Furthermore, the Examiner has failed to identify which feature of Yamanaka is the synchronization apparatus of the subject claims, pointing instead to multiple distinct elements of the reference to represent a single component of the claim. If the Examiner suggests the synchronization apparatus is the master station (or components thereof) then it is readily apparent that the reference does not teach

"configurable to operate as … a synchronization slave." Likewise, if the synchronization apparatus is to be the slave station (or components), a similar deficiency exists. The Examiner is not free to change the definition of the apparatus in order to reject the claim piecemeal. Moreover, in either case, Yamanaka does not contemplate a time synchronization apparatus that is ***configurable***.

In other words, at page 9, the Examiner points to features of Yamanaka's master station (*see* FIG. 3A) to represent a synchronization master of the claimed subject matter, then switches to Yamanaka's slave station (*see* FIG. 3B) to represent a synchronization slave of the claimed subject matter. Thus, the Examiner has done no more than show that Yamanaka teaches ***two distinct components*** existing in a system, one a master and the other a slave. In contrast, independent claim 1 recites a ***single component*** that "*is configurable to operate as* ***both*** a synchronization master and a synchronization slave." In Yamanaka, the master station operates as a master only, but not both, and similarly, the slave station operates only as a slave, but not both. Accordingly, no matter which of these two elements the Examiner chooses to represent the "synchronization apparatus" of claim 1, the analysis fails because neither one can operate as both a master and a slave (and the "either/or" interpretation for the term "both" is not germane as indicated *supra* in §I.). Thus, the Examiner does not in fact cite any portion of Yamanaka to read upon the synchronization apparatus, but merely refers to portions of the reference to indicate the system ***includes*** both a synchronization master and a synchronization slave (as opposed to the synchronization apparatus that can be "***configurable to operate as*** both a synchronization master and a synchronization slave). In fact, Yamanaka teaches no ***configurable*** components.

While the Examiner responds to these arguments, they are not fully considered. For example, when applicants submit that independent claim 1 recites a ***single component*** (*e.g.*, the synchronization apparatus) that "*is configurable to operate as* ***both*** a synchronization master and a synchronization slave," the Examiner responds with the same argument as before citing portions of Yamanaka that teach ***two distinct components***, rather than a single component that can be configurable to operate in two ways. When applicants note Yamanaka fails to disclose a ***configurable*** synchronization apparatus, the Examiner cites the exact same portions of the reference, wherein no configurability is disclosed, but rather two static components. However, to supplement this argument the Examiner posits that Voth teaches these features (*see* Final

Office Action §3.4 at pp. 3-4), which is an inconsistent application of the references, introduced *supra* in §I.

In particular, in response to applicants' remarks that Voth does not include the structure necessary to teach the synchronization apparatus of the independent claims (because the Examiner could not point to a processor interface and/or other components that comprise the synchronization apparatus), the BPAI agreed in the Decision on Appeal (mailed February 9, 2007) and reversed all rejections set forth by the Examiner. Accordingly, it is unequivocally clear that Voth does not teach the synchronization apparatus of the subject claims. Therefore, Voth cannot teach a "synchronization apparatus is configurable…" as recited in the subject claims if for no other reason than that Voth does not disclose a synchronization apparatus in the first place. In other words, it is impossible to disclose a synchronization apparatus that is configurable without at least teaching the synchronization apparatus, which Voth does not do. While applicants do not at this time dispute that Voth can configure a node (*e.g.*, Voth, FIG. 1, elements 102a-d), a node is not the synchronization apparatus. Accordingly, the Examiner is kindly asked to refrain from employing Voth in a manner that readily conflicts with the previous decision by the Board.

For at least the foregoing reasons, it is readily apparent that neither Yamanaka nor Voth teach or suggest the time synchronization apparatus of the subject claims. In the case of Voth, this is self-evident on the record pursuant to the Decision on Appeal, and in the case of Yamanaka, there is no component that can represent ***both*** a master and a slave. Moreover, Yamanaka further provides for no component that is ***configurable***. Therefore, at most, assuming *arguendo* Yamanaka does teach the synchronization component of the subject claims (which the reference does not) and further assuming that Voth discloses configurability (which is not disputed at this time), the combination of Voth and Yamanaka still fails to teach all the claimed features. In particular, in that case, the combination of a synchronization component (Yamanaka) and configurability of components that are decidedly not the synchronization component (Voth) does not read upon claims that recites the "synchronization apparatus is configurable." Accordingly, the Examiner has failed to present a *prima facie* case for obviousness and this rejection with respect to independent claims 1, 38, 39, and 52, as well as all claims that depend there from, should be withdrawn.

Moreover, the Examiner seeks to combine Yamanaka with Voth, yet such a combination does not have a reasonable expectation of success and/or would produce a seemingly inoperative device for at least the following reasons. The method for time synchronization disclosed in Voth relies upon the assumption that the round-trip time between master and slave (transmission delay or latency) is zero. (*See* col. 6, ll. 60-63, where the method performs a round-trip, from the master to the slave and back to the master, then calculates the difference between the time stamps of the master and the slave ***with no offset for the travel time*** of the SYNC message between the two nodes). Although Voth probably understands that instantaneous propagation of the SYNC message is of course impossible, the assumption that the round-trip travel is zero is not necessarily invalid due to the fact that no time difference between clocks is detectable if that difference is less than 1 clock tick. (*See* col. 8, ll. 60-63). Thus, Voth does not care what the actual round-trip time is for the SYNC message as long as the round-trip travel time is less than half of one clock tick, because in that case, the clocks will have the appearance of being synchronized. (*See* col. 8, ll. 64-67).

Hence, the accuracy of the method disclosed in Voth is a function of the speed of the network *versus* the clock frequency of the nodes (*see e.g.*, col. 8, ll. 57-60), and while the round-trip time is assumed to be zero in the synchronization calculation, the ***maximum*** round-trip time must be less than half of 1 tick, or the SYNC message will be rejected terminating the method. (*See* col. 6, ll. 50-53). Thus, the time value of ½ of a tick or clock cycle functions as an upper limit on the accuracy of Voth. (*See* col. 8, ll. 46-49). Therefore, Voth is suitable for SSI computer clusters as disclosed, but is wholly inapplicable to industrial control system networks such as that of Yamanaka or the control system of the subject claims. In contrast, Yamanaka calculates the transmission delay, τ_1, (by averaging the round-trip times) in order to perform synchronization (*see* col. 7, line 32), whereas the "trick" of Voth is to assume this value is zero, but below an upper limit defined by the clock frequency of the master node processor. Accordingly, the combination of Yamanaka and Voth would produce a seemingly inoperative device, which cannot therefore stand as predicates for a *prima facie* case for obviousness.

The Examiner does not appear to fully consider the above rationale, but at page 3 of the Final Office Action, the Examiner relies upon the assumption that technological advances, especially in network speeds can allow Voth to apply to control systems of the subject claims, and also to different time zones by applying Voth to the Internet at large (*see* page 5). However,

both of these arguments are erroneous, as they would require a repeal of accepted laws of nature. To illustrate such and to provide further support for the fact that there is no reasonable expectation of success to combine Voth with Yamanaka, consider the following example:

Today, current processors run at a clock frequency of about 1000 MHz, or about 1 billion ticks per second. It is further known based upon currently accepted physics principles that information cannot be transmitted faster than the speed of light (*e.g.*, 300 million meters per second). Therefore, it can be stated that light will travel about $10^9/3^8 = 3.33$ meters per clock cycle (or tick) or 1.67 meters for every ½ tick. Applying the method of Voth, and assuming the Examiner does not suggest the SYNC message can travel faster than the speed of light, then the round-trip travel distance between 2 nodes must be no greater than 1.67 meters. And since this is a round-trip, the nodes must actually be no greater than 0.835 meters apart, or Voth is guaranteed to exceed the maximum round-trip time, even without any form of network delay. Therefore, even if the synchronization principles recited in Voth and Yamanaka were not mutually exclusive, this example illustrates that Voth cannot be applied to industrial control systems, to systems with different "time zones," to systems that are not a star topology, or to the Internet at large, where nodes could potentially be separated by more than 20 million meters. Thus, quite apart from the Examiner's argument that technological advances can expand the applicability of Voth, such advances have actually rendered the method obsolete, perhaps even in the narrow field of endeavor to which Voth originally applied. Hence, the combination of Yamanaka and Voth does not have a reasonable expectation of success and/or would produce a seemingly inoperative device. Accordingly, the Examiner has failed to present a *prima facie* case for obviousness and this rejection should be withdrawn for yet another reason.

Claims 4-6 and 15-17

Claims 4 and 15 recite a transmitter that periodically transits message frames at a fixed period of 50μs. Voth clearly does not teach this limitation. Rather, Voth merely indicates that messages can be transmitted at fixed intervals, and expressly teaches an update cycle of 20 seconds (*see* col. 9, ll. 20-21), and further teaches that the update cycle *takes about 4 seconds to complete* (*see* col. 8, ll. 21-22). Applicants note that even were it possible for Voth to use a 50μs update cycle (rather than the expressly taught 20 seconds), this would mean that Voth would try to update each node about 80,000 times in the 4 seconds it takes to complete a single update, in

essence spending 80,000 times the resources it costs to do a job once, each and every time and for each and every node. Such a situation defies reason and would be so wasteful of processor and network resources that a single node probably could not ever be properly synchronized, much less a system with many nodes. However, the Examiner attempts to avoid this by blatantly ignoring the claim language. While the claim expressly recites 50μs, the Examiner at page 11 of the Final Office Action points to applicants' specification, noting that although the claim states 50μs, the Examiner is reading this as "some other fixed period" (*e.g.*, such as 20 seconds as Voth teaches), since the specification discloses both. Such analysis is absolutely impermissible. The Examiner is not free to ignore the claimed features of 50μs simply because the specification suggests other intervals are also possible. The claims do not say "or some other fixed period." Instead, the claims state 50μs. Voth expressly teaches only 20 second update cycles and could not be used to suggest any period less than 4 seconds (the duration of the update cycle), let alone 50μs.

Similarly, claims 6 and 17 recite a transmitter transmits a message frame having an LCM indicator at a least common multiple of 600ms. It is readily apparent that Voth does not teach 600ms. Again, the Examiner ignores the plain language of the claim because the specification teaches one in the art that other times can exist. Moreover, regarding claims 5 and 16 (*et al.*), Voth cannot even have an LCM (least common multiple) interval at for at least two reasons: 1) Voth assumes latency between nodes is zero, and therefore all nodes would have a latency of zero, so there is no LCM; 2) Voth only contemplates a star configuration, where all nodes are connected to the master. The Examiner argues at pages 11-12 that the update cycle of Voth is equivalent to the LCM of the claim, however, the Examiner previously argued that Voth's update cycle was the fixed period of claim 4. Clearly, Voth's update cycle cannot simultaneously represent both features of the claim.

Claim 53

Neither Voth nor Yamanaka teach the synchronization apparatus exists in a different synchronization time zone from that of the host processor as recited in dependent claim 53. At pages 28-29 of the Final Office Action, the Examiner argues to the contrary citing Voth at col. 4, ll. 17-19 and suggesting that "distributed internetworking environment such as the Internet operates across time zones." Be that as it may, such a statement has nothing whatever to do with

Voth. Neither at the indicated portions nor anywhere else does Voth teach these features. Rather, Voth is expressly indicated to operate in a high speed TNet, which is not the Internet. Voth cannot function if the network were the Internet due to a latency that would render the method of Voth worthless, as any latency that is greater than half a clock cycles makes Voth inoperable. (*See* col. 8, ll. 60-66). The Internet spans the entire globe, yet even at the speed of light (much less the fastest networks known today), Voth's method of time synchronization would be incapable of functioning at inter-node distances greater than about 0.835 meters. Accordingly, the Examiner's rationale is precluded by well-known natural limits.

III. Rejection of Claims 8-12 Under 35 U.S.C. §103(a)

Claims 8-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka, in view of Voth and Ramussen, *et al*. (US 6,449,732, hereinafter referred to as "Ramussen"). Withdrawal of the rejection is respectfully requested because Yamanaka, Voth, and Ramussen, *et al*., either alone or in combination with one another, do not teach all the claimed features.

In particular, claims 8-12 depend directly or indirectly upon independent claim 1. As noted *supra*, the cited references do not teach or suggest applicants' invention recited in the subject claims. Ramussen, *et al*. fails to make up for the aforementioned deficiencies of Yamanaka and Voth with respect to independent claim 1. Thus, this rejection should be withdrawn.

IV. Rejection of Claims 29, 35-37, and 47 Under 35 U.S.C. §103(a)

Claims 29, 35-37, and 47 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamanaka in view of Voth and in further view of Kuribayashi, *et al*. (US. 6,775,246, hereinafter referred to as "Kuribayashi"). Withdrawal of the rejection is respectfully requested for at least the following reasons. Yamanaka, Voth, and Kuribayashi all fail to teach the all features of the claims, either alone or in combination with one another.

Claims 29, 35-37 depend directly or indirectly upon independent claim 1 while claim 47 depends directly or indirectly upon independent claim 39. As noted *supra*, the Yamanaka and Voth fail to teach or suggest all aspects of the subject claims. Kuribayashi fails to make up for

the aforementioned deficiencies with respect to independent claims 1 and 39. Thus, this rejection should be withdrawn.

Conclusion

The present application is believed to be in condition for allowance in view of the above comments. A prompt action to such end is earnestly solicited.

In the event any fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [ALBRP228US].

Should the Examiner believe a telephone interview would be helpful to expedite favorable prosecution, the Examiner is invited to contact applicants' undersigned representative at the telephone number below.

Respectfully submitted,

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